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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,234	PRALL, KIRK	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,15,16,20-36 and 69-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-9,15,16 and 20-25* is/are allowed.

6)☒ Claim(s) *10-12,26-28,34-36 and 69-77* is/are rejected.

7)☒ Claim(s) *29-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 10-12, 26-28, 34, 35, 36, and 69-77 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> **The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.**

3. Claim 34 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. The examiner is unable to find the portion of the specification which describes the drain as being doped with boron.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 10-12, 26-28, 35, and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong (USPN 5,386,132).

7. With regard to claim 10, Wong (USPN 5,386,132) discloses a similar device. Figure 14E of Wong illustrates a memory cell. There is a first transistor with a source (1402), a drain (1404), and a gate (1435, 1437, 1439). The source (1402) and drain (1404) are arranged substantially vertically. The gate (1435, 1437, 1439) is horizontally positioned such that at least a portion of the gate (1435) overlies at least a portion of the drain (1404). A select transistor is coupled to the first transistor. The select transistor has a source (1402), a drain (1404), and a gate (1409). The select transistor gate (1409) is substantially vertical and perpendicular to the gate (1409) of the first transistor relative to a vertical plane. Wong makes it clear that this particular embodiment has a feature size of $4F^2$ (column 12, lines 51-60); which is less than $4.5F^2$.

8. In reference to claim 11, the source of the first transistor (1402) has an upper surface which is located below the lower surface of the first transistor drain (1404).

9. With regard to claim 12, the source (1402) and the drain (1404) are shared by the first transistor and the select transistor.

10. In reference to claim 26, Wong (USPN 5,386,132) discloses a similar device. Figure 14E of Wong illustrates a memory device with a first n-type source layer (1402) formed over a substrate (1401). There is a p-type layer (1403) over the n-type layer (1402). A second n-type drain layer (1404) is formed in the p-type layer (1403). A select trench is formed in the p-type layer (1403). There is a substantially vertical select

gate (1409) formed in the select trench. A floating gate (1435, 1437, 1439) is formed over the p-type layer (1403) so as to avoid the select trench.

11. With regard to claim 27, a tunnel oxide (1434) is formed over the substrate (1401).

12. In reference to claim 28, the select gate (1409) is the wordline. As seen in figure 13, there are digitlines or bitlines over the substrate.

13. In reference to claim 35, the floating gate (1435, 1437, 1439) is formed of polysilicon and has a tunnel oxide (1434). Although not labeled, there are oxide layers on the left and right of the floating gate (1435, 1437, 1439).

14. With regard to claim 36, the applicant describes the floating gate as being "self-aligned." The applicant has defined a "self-aligned gate" as a gate which is formed before the source/drain diffusions are made (p.19, lines 11-13). This places claim 36 into the form of a **product-by-process claim**:

> Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe,* 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi* et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 36 does not distinguish over the Wong reference regardless of the process order used to form the floating gate and the source/drain diffusions, because only the final product is relevant, and not the process of making such as forming the gate before the source/drain diffusions are made.

15. Claims 69-77 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong (USPN 5,386,132).

16. With regard to claim 69, Wong (USPN 5,386,132) discloses a similar device. Figure 6 of Wong illustrates a memory device with a substrate (601). There is a buried source (602) formed in the substrate (601). A first layer (603) is formed over the substrate (601). A first drain is in the first layer (603) which is generally over the buried source (602) which defines a first substantially vertical channel between them. There is a trench formed in the first layer (603). There is a select gate (609) formed in the trench. A first floating gate (605) is formed over the first layer (603) adjacent to the trench and proximate to the first substantially vertical channel.

17. In reference to claim 70, there is a second drain (604) formed in the first layer (603) which is generally over the buried source (602) which defines a second substantially vertical channel between them. A second floating gate (605) is formed over the first layer (603) adjacent to the trench and proximate to the second substantially vertical channel.

18. With regard to claim 71, the floating gate (605) defines a horizontal floating gate (605) arranged over the first layer (603) such that at least a portion of the floating gate (605) overlies at least a portion of the drain (604).

19. In reference to claim 72, the floating gate (605) defines a horizontal floating gate (605) further arranged generally above the substantially vertical channel.

20. With regard to claim 73, the trench extends through the first layer (603) to the buried source (602).

21. With regard to claim 74, Wong (USPN 5,386,132) discloses a similar device. Figure 6 of Wong illustrates a memory device with a first layer (602) defining a source. A second layer (603) is formed over the first layer (603). A drain (604) is in the second layer (603) which is generally over the source (602) which defines a substantially vertical channel between them. There is a trench formed in the second layer (603). There is a select gate (609) formed in the trench. A floating gate (605) is formed over the second layer (603) adjacent to the trench.

22. With regard to claim 75, the floating gate (605) defines a horizontal floating gate (605) arranged over the second layer (603) such that at least a portion of the floating gate (605) overlies at least a portion of the drain (604).

23. With regard to claim 76, the trench extends through the second layer (603) and into the first layer (602).

24. In reference to claim 77, the floating gate (605) defines a horizontal floating gate (605) further arranged generally above the substantially vertical channel.

25. Claims 74-77 are rejected under 35 U.S.C. 102(b) as being anticipated by Mori (USPN 5,576,567).

26. With regard to claim 74, Mori (USPN 5,576,567) discloses a similar device. Figures 1a and 1b of Mori illustrate a memory device with a first layer (23, 32) defining a source. A second layer (36) is formed over the first layer (23, 32). A drain (24) is in the second layer (36) which is generally over the source (23, 32) which defines a substantially vertical channel between them. There is a trench formed in the second

layer (36). There is a select gate (38) formed in the trench. A floating gate (FG) is formed over the second layer (36) adjacent to the trench.

27. With regard to claim 75, the floating gate (FG) defines a horizontal floating gate (FG) arranged over the second layer (36) such that at least a portion of the floating gate (FG) overlies at least a portion of the drain (24).

28. With regard to claim 76, the trench extends through the second layer (36) and into the first layer (23, 32).

29. In reference to claim 77, the floating gate (FG) defines a horizontal floating gate (FG) further arranged generally above the substantially vertical channel.

Allowable Subject Matter

30. Claims 1-9, 15, 16, and 20-25 are allowed.

31. Claims 29-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

32. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a non-volatile semiconductor memory device with two transistors which has a vertical channel (with the drain over the source), a floating gate over the drain, a select gate within a trench, and a feature size less than $4F^2$.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
May 4, 2003

NATHAN J. FLYNN
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